Exploring Soft ECC Decoding

Growing interest for software Error Correction Codes implementations
- Leverage powerful, energy efficient pros.
- Reduce dev. cost and time to market
- Validate and optimize new algorithms

Recent Successive Cancellation soft decoders for Polar ECC codes strongly benefit from modern CPUs capabilities and SIMD units, open the way to a wide optimization range.

Introducing P-EDGE, an environment for exploring Polar ECC decoders.
- Specialized skeleton generator
- Building blocks library

Decoding of Polar Codes

The Successive Cancellation (SC) decoding algorithm: a depth-first tree traversal algorithm based on 3 key functions:
\[
\begin{align*}
    f(\lambda_0, \lambda_1) &= \text{sign}(\lambda_0 - \lambda_1) \cdot \min(|\lambda_0|, |\lambda_1|) \\
    g(\lambda_0, \lambda_1, s) &= (1 - 2s)\lambda_1 + \lambda_0 \\
    h(\lambda_0, \lambda_1) &= (\lambda_0 \oplus \lambda_1, s_0, s_1).
\end{align*}
\]

Figure 1: Per-node downward and upward computations

Results

Fig. 2 shows the performance of the P-EDGE generated decoders on various SIMD strategies and on an Intel® Xeon® E31225 CPU @ 3.1GHz (Sandy Bridge architecture). Higher is better.

Figure 2: 32-bit floating point intra frame performance comparison: the two cross marks show state-of-the art performance results reported in [1] (left); 8-bit fixed point performance comparison: circles show P-EDGE results and triangles show our former “handwritten” implementation results [2] (right).

The P-EDGE exploration capabilities are demonstrated on Fig. 3: various optimizations can have different impacts on the performance depending on the code rate and the SIMD strategy we use.

Figure 3: Throughput depending on the different optimizations (frame size \(N = 2048\)), for intra-frame vectorization on the left and intra-frame vectorization on the right, resp. Compression techniques disabled.